REVISIONS

LTR	DESCRIPTION	DATE(YR-MO-DA)	APPROVED
A	Add three vendors, 18324, 1FN41, and 66579. Add device types 04, 05, 06, and 07. Add margin test method C. Update vendor's PIN. Change code indent. no. to 67268. Editorial changes throughout.	87-12-17	M. A. Frye
B	Add device type 08 with vendors CAGE 1FN41 and CAGE 66579. Added time temperature regression equation for unbiased bake. Removed vendor CAGE 66302. Made technical changes to table I, 4.2 back end margin test method step 3, 4.3.1 step C, table II, and table III. Editorial changes throughout. Added vendor's PIN from XMB/883 to either_ LM/883 for appropriate device types. Deleted the top CE waveform on figure 6. This was incorrect for this device.	90-12-05	M. A. Frye
C	Added vendor CAGE 34335 to the drawing as a source of supply for device types 01 through 07. Add vendor CAGE number 66579 to device types 01 through 04, also add vendor CAGE number 01295 to devices 04xx and 05xx. Add test condition A to 4.2 and 4.3.2. Add margin test method E for vendor CAGE number 34335. Change to figure 3, margin test method C for vendor CAGE 01295 and change to programming waveforms. Change to 4.5. Editorial changes throughout. Add case outline Z for vendor CAGE number 1FN41.	90-01-30	M. A. Frye
D	Changes in accordance with NOR 5962-R130-92.	92-01-30	M. A. Frye
E	Add case outline U. Add device types 09 and 10. Remove vendor 27014 from drawing. Editorial changes throughout.	93-10-15	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	E	E	E	E	E															
SHEET	14	15	16	17	18															

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
James E. Jamison

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-02-12

REVISION LEVEL
E

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 262,144-BIT UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	86063
A	14933	

SHEET 1 OF 18

DESC FORM 193-1
JUL 91

5962-E384-93

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-86063	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	(see 6.6)	32K x 8-bit UV EPROM	200 ns
02	(see 6.6)	32K x 8-bit UV EPROM	250 ns
03	(see 6.6)	32K x 8-bit UV EPROM	300 ns
04	(see 6.6)	32K x 8-bit UV EPROM	170 ns
05	(see 6.6)	32K x 8-bit UV EPROM	150 ns
06	(see 6.6)	32K x 8-bit UV EPROM	120 ns
07	(see 6.6)	32K x 8-bit UV EPROM	90 ns
08	(see 6.6)	32K x 8-bit UV EPROM	70 ns
09	(see 6.6)	32K x 8-bit UV EPROM	55 ns
10	(see 6.6)	32K x 8-bit UV EPROM	45 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line 1/
Y	CQCC1-N32	32	Dual-in-line 1/
Z	See figure 1	32	J-lead chip carrier 1/
U	CDIP3-T28 or GDIP4-T28	28	Dual-in-line 1/

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Storage temperature - - - - - - - - - - - - - - - - - -65°C to +150°C
Input voltages with respect to ground - - - - - - - +6.5 V dc to -0.3 V dc
Output voltages with respect to ground - - - - - - V_{CC} +0.3 V dc to GND -0.3 V dc
V_{PP} supply voltage with respect to ground - - - - - +14.0 V dc to -0.6 V dc
Power dissipation (P_D) 2/ - - - - - - - - - - - - - - +500 mW
Lead temperature (soldering, 10 seconds)- - - - - - +300°C
Thermal resistance, junction-to-case (Θ_{JC}):
  Case outlines X, Y, and U - - - - - - - - - - - - - See MIL-STD-1835
  Case outline Z - - - - - - - - - - - - - - - - - - - 13°C/W
Junction temperature (T_J) - - - - - - - - - - - - - - +150°C

1.4 Recommended operating conditions.

Case operating temperature (T_C) - - - - - - - - - - -55°C to +125°C
Supply voltage (V_{CC})- - - - - - - - - - - - - - - - +4.5 V dc to +5.5 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Block diagram. The block diagram shall be as specified on figure 3.

3.2.3 Truth table. The truth table shall be as specified on figure 4.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 4.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical test for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of state of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input load current	I_{LI}	V_{IN} = 0 to 5.5 V	All	1, 2, 3		±10	µA
Output leakage current	I_{LO} 1/	V_{OUT} = 0 to 5.5 V	All	1, 2, 3		±10	µA
Operating current TTL inputs	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$ 0_{0-7} = 0 mA $f = \frac{1}{t_{ACC}}$ maximum	01-05 06 07 08 09 10	1, 2, 3		50 65 70 90 115 130	mA
Operating current CMOS inputs	I_{CC2}	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$ 0_{0-7} = 0 mA $f = \frac{1}{t_{ACC}}$ maximum	01,02, 03 04,05 06 07 08,09 10	1, 2, 3		25 40 55 60 90 100	mA
Standby current TTL inputs	I_{SB1}	$\overline{CE} = V_{IH}$ V_{CC} = 5.5 V, f = ϕ	01-05 06,07, 08,09, 10	1, 2, 3		3 5 45	mA
Standby current CMOS inputs	I_{SB2}	$\overline{CE} = V_{IH}$ V_{CC} = 5.5 V, f = ϕ	01-07, 08,09, 10	1, 2, 3		300 45	µA mA
V_{PP} read current	I_{PP}	$V_{PP} = V_{CC}$ = 5.5 V	All	1, 2, 3		200	µA
Input low voltage (TTL) (±10 percent supply)	V_{IL1} 2/	$V_{PP} = V_{CC}$	All	1, 2, 3	-0.1 3/	0.8	V
Input low voltage (CMOS)	V_{IL2} 2/	$V_{PP} = V_{CC}$	All	1, 2, 3	-0.2 3/	0.2	V
Input high voltage (TTL) (±10 percent supply)	V_{IH1} 2/	$V_{PP} = V_{CC}$	All	1, 2, 3	2.0	V_{CC} +1.0 3/	V
Input high voltage (CMOS)	V_{IH2} 2/	$V_{PP} = V_{CC}$	All	1, 2, 3	V_{CC} -0.2	V_{CC} +0.2 3/	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output low voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = 5.5 V	All	1, 2, 3		0.45	V
Output high voltage	V_{OH}	I_{OH} = -400 µA	All	1, 2, 3	2.4		V
Output short circuit current	I_{OS} 3/ 4/		All	1, 2, 3		-100	mA
V_{PP} read voltage	V_{PPR}		All	1, 2, 3	V_{CC} -0.7	V_{CC}	V
Address to output delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} 5/ 6/	01	9, 10, 11		200	ns
			02			250	
			03			300	
			04			170	
			05			150	
			06			120	
			07			90	
			08			70	
			09			55	
			10			45	
$\overline{CE}$ to output delay	t_{CE}	$\overline{OE}$ = V_{IL} 5/ 6/	01	9, 10, 11		200	ns
			02			250	
			03			300	
			04			170	
			05			150	
			06			120	
			07			90	
			08			70	
			09			55	
			10			45	
$\overline{OE}$ to output delay	t_{OE}	$\overline{CE}$ = V_{IL} 5/ 6/	01	9, 10, 11		75	ns
			02			100	
			03			150	
			04,05			70	
			06,08			35	
			07			30	
			09			25	
			10			20	
$\overline{OE}$ high to output float	t_{DF} 3/	$\overline{CE}$ = V_{IL} 5/ 6/	01	9, 10, 11	0	55	ns
			02			60	
			03			105	
			04,05			50	
			06,08			35	
			07			30	
			09			25	
			10			20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output hold from addresses CE or $\overline{OE}$ (whichever occurred first)	t_{OH} 3/	$\overline{CE} = \overline{OE} = V_{IL}$ 5/ 6/	All	9, 10, 11	0		ns
Input capacitance	C_{IN} 7/	$V_{IN} = 0\ V$ $f = 1\ MHz$ See 4.3.1c	All	4		12	pF
Output capacitance	C_{OUT} 7/	$V_{OUT} = 0\ V$ $f = 1\ MHz$ See 4.3.1c	All	4		14	pF
Functional tests		See 4.3.1e	All	7,8A,8B			

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{LO} with the output under test connected to V_{OUT}.
2/ Tests for all input and control pins.
3/ Guaranteed if not tested.
4/ V_{PP} may be one diode drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and be removed simultaneously or after V_{PP}.
5/ See figures 5 and 6.
6/ Equivalent ac test conditions (actual load conditions vary by tester):
Output load: 1 TTL gate and $C_L = 100$ pF.
Input rise and fall times $\le$ 20 ns.
Input pulse levels: 0.45 V and 2.4 V.
Timing measurement reference levels:
Inputs = 0.8 V and 2.0 V.
Outputs = 0.8 V and 2.0 V.
7/ All pins not being tested are to be grounded.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

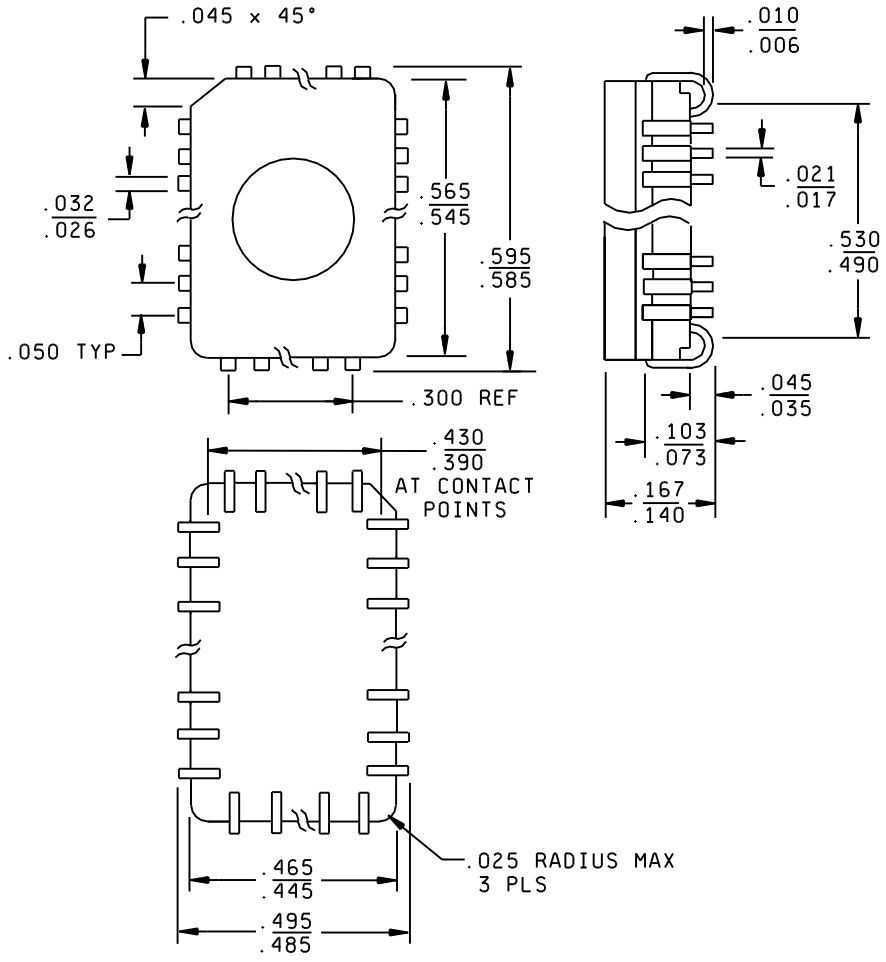
a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

Case Z



Inches	mm
.006	0.15
.010	0.25
.017	0.43
.021	0.53
.025	0.63
.026	0.66
.032	0.81
.035	0.89
.045	1.14
.050	1.27
.073	1.85
.103	2.62
.140	3.56
.167	4.24
.300	7.62
.390	9.90
.430	10.90
.445	11.36
.465	11.83
.485	12.34
.490	12.40
.495	12.67
.530	13.53
.545	13.81
.565	14.46
.585	14.97
.595	15.11

FIGURE 1. 32-lead, windowed ceramic J-leaded chip carrier (JLCC).

Device types	01-10	
Case outlines	X, U	Y, Z
Terminal number	Terminal symbol	
1	V_{PP}	NC
2	A_{12}	V_{PP}
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_0	A_1
11	O_0	A_0
12	O_1	NC
13	O_2	O_0
14	GND	O_1
15	O_3	O_2
16	O_4	GND
17	O_5	NC
18	O_6	O_3
19	O_7	O_4
20	$\overline{CE}$	O_5
21	A_{10}	O_6
22	$\overline{OE}$	O_7
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}$
26	A_{13}	NC
27	A_{14}	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	A_{13}
31	---	A_{14}
32	---	V_{CC}

NC = no connection

FIGURE 2. Terminal connections.

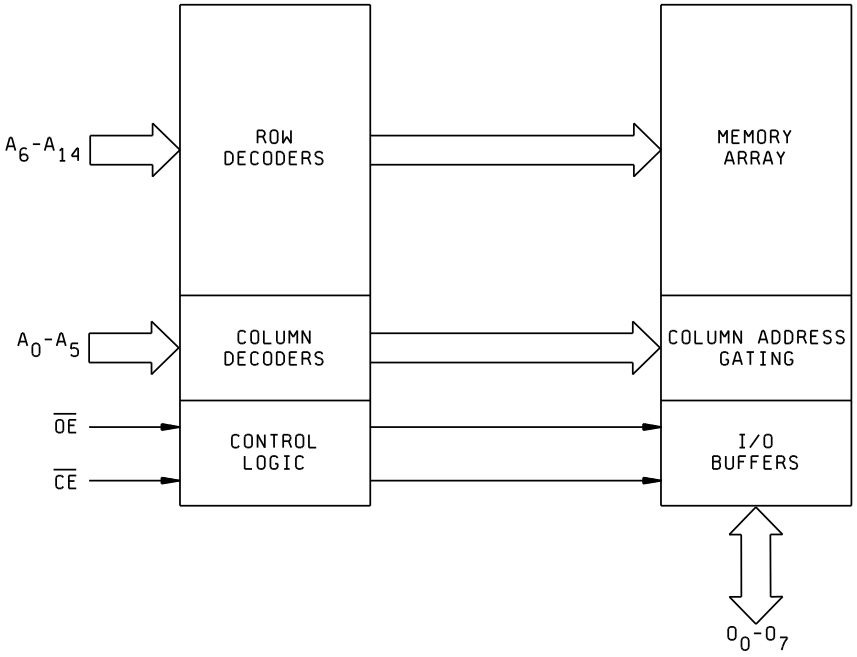


FIGURE 3. Block diagram.

Mode	$\overline{CE}$	$\overline{OE}$	V_{PP} 2/	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X 1/	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP} 2/	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP} 2/	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP}	High Z

1/ X can be either V_{IL} or V_{IH}.

2/ For V_{PP} see 4.5.

FIGURE 4. Truth table.

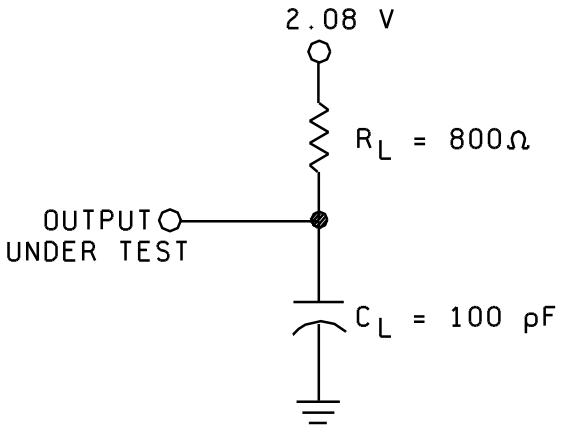
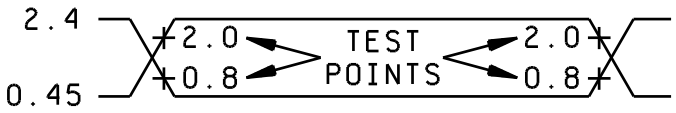


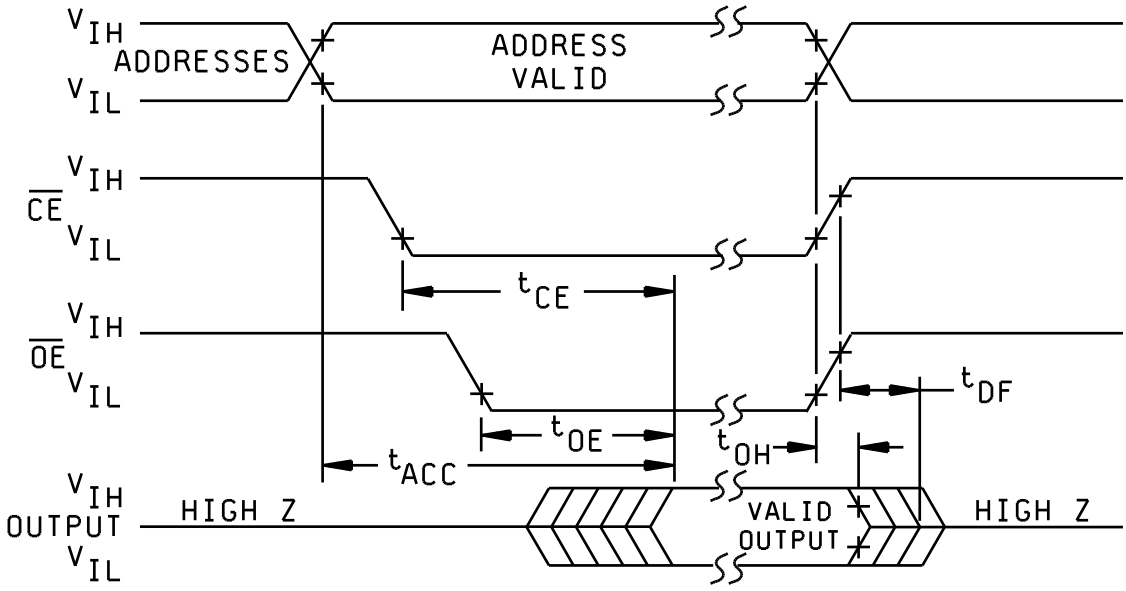
FIGURE 5. **Output load circuit**.

AC TESTING INPUT, OUTPUT WAVEFORM



AC TESTING: INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.45 FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0".

AC WAVEFORMS



NOTES:
1. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

FIGURE 6. Switching waveforms.

Margin test method A:

(1) Program at +25°C with a greater than 95 percent pattern (example, diagonal "1's") (see 3.6.2).

(2) Unbiased bake for 8 hours at +200°C or 24 hours at +170°C or 72 hours at +150°C.

(3) Test at +95°C (see 3.6.3), including a margin test at V_m = +6 V and loose timing (i.e., t_{ACC} = 1 µs).

(4) Erase (see 3.6.1).

(5) Program at +25°C with a 50 percent pattern (example, checkerboard bar) (see 3.6.2). (Programmed with checkerboard at wafer sort).

(6) Test at +125°C (see 3.6.3).

(7) Burn-in (see 4.2a).

(8) Test at +125°C (see 3.6.3).

(9) Test at -55°C (see 3.6.3).

(10) Erase (see 3.6.1). Devices may be submitted for groups A, B, C, and D testing at this point.

(11) Verify erasure at +25°C (see 3.6.3).

Margin test method B: * Steps 1 through 3 may be performed at wafer level. The maximum unbiased bake temperature should not exceed +200°C for packaged devices or +300°C for unassembled devices.

*(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.6.2). The remaining cells shall provide a worst case speed pattern.

*(2) Bake,unbiased, for 72 hours at +140°C. or 72 hours at +225°C (unassembled devices only).

*(3) Perform a margin test using V_m = +5.8 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = 5.8 V at +25°C.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.6.1). Devices may be submitted for groups A, B, C, and D testing at this point.

(8) Verify erasure (see 3.6.3).

Margin test method C:

Wafer margin test method:

(1) Program at +25°C with a greater than 95 percent pattern (example, all "0's").

(2) Measure V_{CC} maximum and store in die signature row.

(3) Unbiased bake for 2 hours at +250°C.

(4) Test at +25°C. Measure V_{CC} maximum and compare to V_{CC} maximum stored in die. Any die with a delta greater than 0.66 V constitutes a failure and is removed from the lot.

Back end margin test method:

(1) Program at +25°C with a greater than 95 percent pattern (example, all "0's") (see 3.6.2).

(2a) Test at +25°C. (8.0 V > V_{CC} maximum range > 6.0 V). Measure and record V_{CC} maximum in signature row. Unbiased bake for 32 hours at +200°C or:

(2b) Test at +25°C. (8.0 V > V_{CC} maximum range > 6.2 V). Measure and record V_{CC} maximum in signature row. Unbiased bake for 48 hours at +165°C.

(3) The storage time may be modified by using other temperatures in accordance with the Arrehenius relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e., °C + 273 = °K).
t_1 = time (hours) at temperature T_1.
t_2 = time (hours) at temperature T_2.
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.
The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(4) Test at +25°C (see wafer margin, step 4 above).

(5) Erase (see 3.6.1).

(6) Program at +25°C with a 50 percent pattern (example, checkerboard bar) (see 3.6.2).

(7) Test at +25°C (see 3.6.3).

(8) Burn-in (see 4.2a).

(9) Test at +25°C (see 3.6.3).

(10) Test at +125°C (see 3.6.3).

(11) Test at -55°C (see 3.6.3).

(12) Erase (see 3.6.1). Devices may be submitted for groups A, B, C, and D testing at this point.

(13) Verify erasure at +25°C (see 3.6.3).

Margin test method D: Steps 1 through 4 are performed at wafer level.

(1) Program at +25°C 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C.

(3) Perform margin test at V_m = 5.9 V.

(4) Erase (see 3.6.1).

(5) Perform interim electrical tests.

(6) Program with checkerboard pattern and verify (see 3.6.2).

(7) Perform dynamic burn-in (see 4.2a).

(8) One-hundred percent test at +25°C (group A, subgroups 1 and 7). V_m = 5.9 V with loose timing, apply PDA.

(9) Perform remaining final electrical subgroups and group A testing.

(10) Erase, devices may be submitted for groups B, C, and D at this time.

(11) Verify erasure (see 3.6.3).

Margin test method E:

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.6.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 24 hours at +200°C or equivalent.

(3) Perform a margin test using Vm = +5.8 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Erase (see 3.6.1).

(5) Program at +25°C with a checkerboard pattern (see 3.6.2).

(6) Program dynamic burn-in (see 4.2a).

(7) Margin at Vm = +5.8 V at +25°C.

(8) Perform electrical test (see 4.2).

(9) Erase (see 3.6.1) Devices may be submitted for groups A, B, C, and D testing at this point.

(10) Verify erasure (see 3.6.3).

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4***, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

1/ * indicates PDA applies to subgroups 1 and 7.
2/ ** indicates that subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.
3/ *** See 4.3.1c.
4/ Any subgroups at the same temperature may be combined when using a multifunction tester.
5/ Subgroups 7 and 8 shall consist of verifying the applicable data pattern, see 4.3.1e.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 shall include verification of the pattern specified in 4.3.1d.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-10-15

Approved sources of supply for SMD 5962-86063 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar 1/ PIN
5962-8606301XX	34649	MD27C256-20/B
	61394	DM27C256-200
	01295	SMJ27C256-20JM
	18324	27C256/BXA-20
	1FN41	AT27C256R-20DM/883
	34335	AM27C256-200/BXA
	66579	WS27C256L-20DMB
5962-8606301YX	18324	27C256/BUA-20
	61394	LM27C256-200
	1FN41	AT27C256R-20LM/883
	34649	MR27C256-20/B
	34335	AM27C256-200/BUA
	66579	WS27C256L-20CMB
5962-8606301ZX	1FN41	AT27C256R-20KM/883
5962-8606301UX	66579	WS27C256L-20TMB
5962-8606302XX	34649	MD27C256-25/B
	61394	DM27C256-250
	01295	SMJ27C256-25JM
	18324	27C256/BXA-25
	1FN41	AT27C256R-25DM/883
	34335	AM27C256-250/BXA
	66579	WS27C256L-25DMB
5962-8606302YX	18324	27C256/BUA-25
	61394	LM27C256-250
	1FN41	AT27C256R-25LM/883
	34649	MR27C256-25/B
	34335	AM27C256-250/BUA
	66579	WS27C256L-25CMB
5962-8606302ZX	1FN41	AT27C256R-25KM/883
5962-8606303XX	61394	DM27C256-300
	01295	SMJ27C256-30JM
	1FN41	AT27C256R-30DM/883
	34335	AM27C256-300/BXA
	66579	WS27C256L-30DMB

See footnote at end of table.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar 1/ PIN
5962-8606303YX	61394	LM27C256-300
	1FN41	AT27C256R-30LM/883
	34335	AM27C256-300/BUA
	66579	WS27C256L-30CMB
5962-8606303ZX	1FN41	AT27C256R-30KM/883
5962-8606304XX	1FN41	AT27C256R-17DM/883
	34335	AM27256-170/BXA
	34649	MD27C256-17/B
	66579	WS27C256L-17DMB
	01295	SMJ27C256-17JM
5962-8606304YX	1FN41	AT27C256R-17LM/883
	34335	AM27C256-170/BUA
	34649	MR27C256-17/B
	66579	WS27C256L-17CMB
5962-8606304ZX	1FN41	AT27C256R-17KM/883
5962-8606304UZX	66579	WS27C256L-15TMB
5962-8606305XX	1FN41	AT27C256R-15DM/883
	66579	WS27C256L-15DMB
	34335	AM27C256-150/BXA
	34649	MD27C256-15/B
	01295	SMJ27C256-15JM
5962-8606305YX	1FN41	AT27C256R-15LM/883
	66579	WS27C256L-15CMB
	34335	AM27C256-150/BUA
	34649	MD27C256-15/B
5962-8606305ZX	1FN41	AT27C256R-15KM/883
5962-8606305UX	66579	WS27C256L-12TMB
5962-8606306XX	1FN41	AT27C256R-12M/883
	66579	WS27C256L-12DMB
	34335	AM27C256-120/BXA

See footnote at end of table.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar 1/ PIN
5962-8606306YX	1FN41 66579 34335	AT27C256R-12LM/883 WS27C256L-12CMB AM27C256-120/BUA
5962-8606306ZX	1FN41	AT27C256R-12KM/883
5962-8606307XX	1FN41 66579 34335	AT27C256R-90DM/883 WS27C256L-90DMB AM27C256-90/BXA
5962-8606307YX	1FN41 66579 34335	AT27C256R-90LM/883 WS27C256F-90CMB AM27C256-90/BUA
5962-8606307ZX	1FN41	AT27C256R-90KM/883
5962-8606308XX	66579 1FN41	WS57C256F-70DMB AT27C256R-70DM/883
5962-8606308YX	66579 1FN41	WS57C256F-70CMB AT27C256R-70LM/883
5962-8606308ZX	1FN41	AT27C256R-70KM/883
5962-8606309XX	66579	WS57C256F-55DMB
5962-8606309YX	66579	WS57C256F-55CMB
5962-8606309UX	66579	WS57C256F-55TMB
5962-8606310XX	66579	WS57C256F-45DMB
5962-8606310YX	66579	WS57C256F-45CMB
5962-8606310UX	66579	WS57C256F-45TMB

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Margin test method
01295	Texas Instruments, Incorporated 13500 North Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland TX 79711-0448	C
1FN41	Atmel Corporation 2125 O'Nel Drive San Jose, CA 95131	B
18324	Signetics Corporation 1275 South 800 East Street Orem, UT 84058 Point of contact: 811 East Arques Avenue Sunnyvale, CA 94088-3409	D
34335	Advanced Micro Devices 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	E
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 West Williams Field Road Chandler, AZ 85224	B
61394	Seeq Technology 47131 Bayside Parkway Fremont, CA 94538	A
66579	Waferscale Integration, Incorporated 47280 Kato Road Fremont, CA 94538	A